Lightly Doped Emitter HBT for Low-Power Circuits

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***Abstract*—We report an approach to reduce the base–emitter capacitance in AlGaAs/GaAs heterojunction bipolar transistors (HBT's) by adding a lightly doped emitter (LDE) region together with appropriate planar (δ) doping region to a conventional base–emitter junction. This improves both the f_t and β for low collector current density (J_c) operation while preserving the high peak f_t at high J_c. When applied to a current mode logic 128/129 programmable prescaler, the LDE HBT results in a reduction in power dissipation and improved bandwidth without any circuit modifications.**

***Index Terms*— Frequency conversion, heterojunction bipolar transistor, MMIC's.**

I. Introduction

AlGaAs/GaAs-BASED heterojunction bipolar transistors (HBT's) are being applied in a variety of microwave and high-speed digital circuits. Typically, HBT's are biased at high collector current densities for high speed, requiring relatively high power dissipation. However, the maximum device speed might not always be needed throughout the entire design. In such cases, the development of high-speed low-power HBT's can increase the attractiveness of HBT technology. Applications can include portable wireless communications, moderate power digital circuits, and A/D converters. In this letter, the performance of a low-power high-speed HBT is discussed. The low-power attributes of these HBT's are demonstrated in a digital circuit fabricated with TRW's baseline microwave HBT process.

II. Device Results

The transit time (τ_{ec}) of an HBT is expressed as follows [1]:

$$\tau_{ec} = \frac{1}{2\pi f_t} = \frac{kT}{qJ_c}\left[C_{be,dep} + C_{bc}\right] + \tau_b + \tau_{cslc} + C_{bc}[R_e + R_c].$$

Here $C_{be,dep}$ is the depletion capacitance of the base–emitter junction and other symbols are standard. At high current densities ($J_c \approx 5\times10^4$ A/cm^2), near the peak f_t bias, the base (τ_b) and the collector space charge layer (τ_{cslc}) transit times limit f_t. At low current density ($10^2 < J_c < 10^4$ A/cm^2), $C_{be,dep}/g_m$ dominates τ_{ec}. Reducing C_{be} would increase f_t at low J_c, improving HBTs' microwave performance at lower bias.

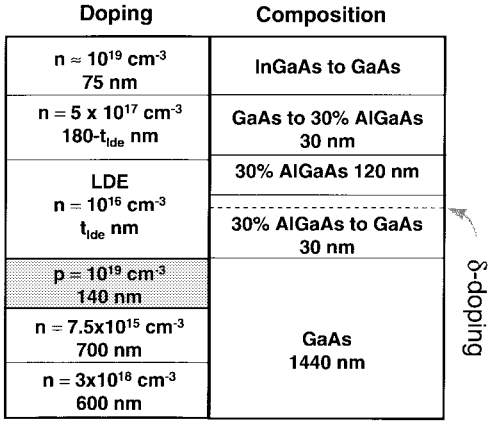

Fig. 1. LDE HBT epilayer structure.

In this work, TRW baseline HBT's [2] were modified for low-power high-speed operation. The base–emitter capacitance was reduced by increasing the depletion region width with a fully depleted lightly doped emitter (LDE) layer placed between the base and the emitter of the baseline HBT, as shown in Fig. 1. The standard TRW HBT process was used to fabricate the devices. With an LDE thickness of 137 nm doped n-type to 10^{16} cm^{-3}, C_{be} at typical forward biases can be reduced by as much as 2.7×, leading to increased f_t at low J_c [3] as shown in Fig. 2(a). The 137-nm LDE design can improve f_t by as much as 2.3× at low J_c. The microwave performance of the 100-nm design is similar.

The dc current gain (β) of the initial LDE devices is lower than that of the baseline HBT's. Simulations show that the LDE introduces a potential barrier in the conduction band whose height above the base E_c will be referred to as ΔE_c [3]. ΔE_c retards electron flow and the corresponding valence band shift favors hole injection into the emitter, thus ΔE_c reduces β and increases the base–emitter turn-on voltage ($V_{be,on}$). The β of the 137-nm-LDE only device, as shown in Fig. 2(b), is much lower than the baseline HBT.

The negative side effects in the thick LDE AlGaAs/GaAs HBT's can be countered by band profile shaping with δ-doping [3]. Using δ-doping of Si donors around 6×10^{11} cm^{-2} near the conduction band barrier maximum, ΔE_c can be lowered by as much as 60 meV [3]. The location of the maximum

Manuscript received July 15, 1997. This work was supported in part by ARPA under the MIMIC Phase 3 program (Contract DAAL-01-92-K-0262) and was monitored by the Army Research Laboratory, Fort Monmouth, NJ.

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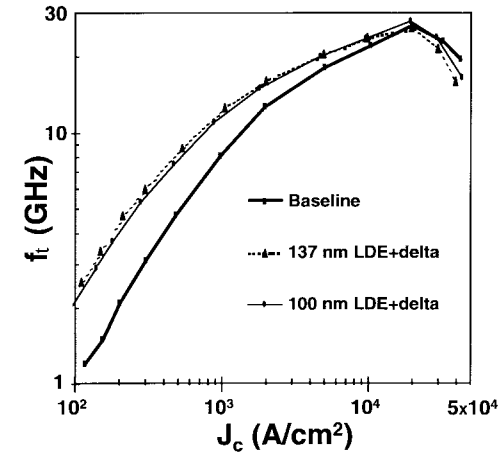
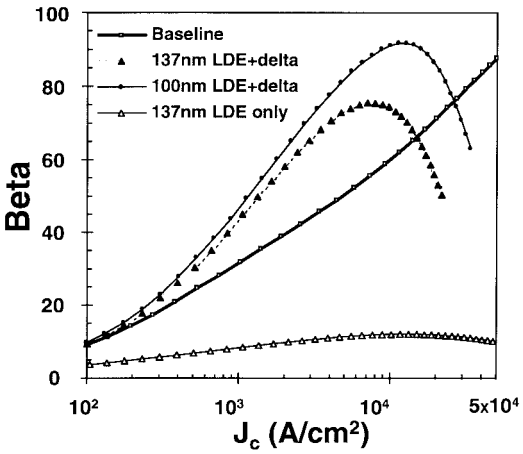
Publisher Item Identifier S 1051-8207(97)08186-5.



(a)



(b)

Fig. 2. (a) Measured f_t versus J_c for a quad 2 × 10 μm^2 and (b) measured β versus J_c for a 2 × 5 μm^2.

ΔE_c occurs near the AlGaAs to graded-AlGaAs interface 300 Å from the base (Fig. 1). The reduced ΔE_c minimizes the LDE induced increase in $V_{be,on}$ and increases the hole barrier for increased β. The small remaining ΔE_c tends to reduce recombination in the base–emitter space charge region, leading to higher β than the β of the baseline device. In abrupt HBT's without the LDE, it has been shown that δ-doping in the emitter can reduce $V_{be,on}$ and increase β [4]. Fig. 2(b) illustrates the β versus J_c curves of the different designs. All of the δ-doped structures have significantly increased β over the baseline for $J_c < 10^4$ A/cm^2 in addition to higher f_t.

III. Circuit Results

For differential pairs in logic circuits, the performance limiting average input capacitance can be expressed as

$$\langle C_{in} \rangle = \frac{Q_{in}}{\Delta V_{logic}} = C_{be} + 2C_{bc} + \frac{\tau_f}{R_{load}}.$$

Q_{in} is the total input charge, ΔV_{logic} is the logic swing, τ_f is the forward transit time (related to the diffusion capacitance), and R_{load} is the differential pair load resistance. At low bias, C_{be} represents 80% of $\langle C_{in} \rangle$ with the baseline (microwave) HBT. In the 137-nm LDE HBT, $\langle C_{in} \rangle$ is reduced by 1.9× [3].

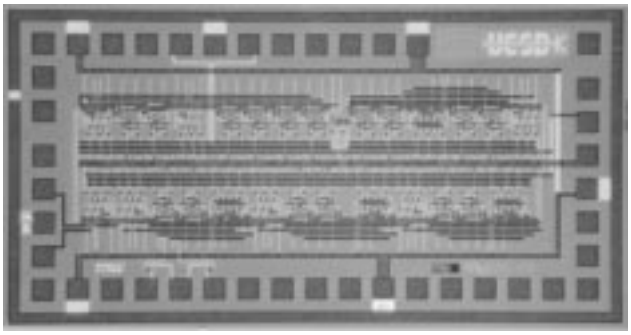


Fig. 3. Photograph for the fabricated prescaler.

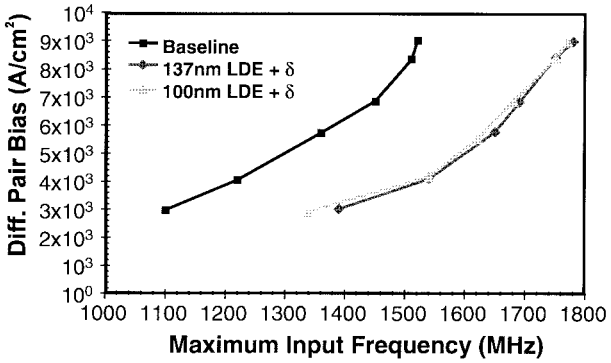


Fig. 4. Differential pair bias versus maximum input frequency of the prescaler.

With lower $\langle C_{in} \rangle$, similar performance can be expected with lower power dissipation.

A two-level CML divide-by-128/129 prescaler was chosen as the LDE HBT demonstration vehicle. The prescaler topology consists of a programmable divide by 4/5 cascaded with a 5-bit counter. The load resistance is 330 Ω and the bias is variable.

In this work, the prescaler was implemented with the TRW monolithic microwave integrated circuit (MMIC) HBT foundry design rules. The results demonstrate the ability of a microwave process to yield digital circuits with high levels of integration. In the MMIC process, the second layer metal consists of plated gold 3 μm thick for low-loss passive elements. The minimum line and space widths are larger than in a digital process, resulting in increased chip area (by about 3×). In the MMIC process, the smallest HBT has an emitter area of 2 × 5 μm^2 which is larger than for transistors found in a typical digital process, this typically increases P_{diss}. In principle, the standard MMIC process can be modified to lower both P_{diss} and area. However, our objective is to demonstrate the power saving capabilities of the LDE HBT which do not require further area scaling. Fig. 3 contains a photograph of the fabricated prescaler. This chip contains 223 HBT's, fabricated next to several TRW 20-GHz MMIC's, paving the way for combined microwave and digital circuits.

Prescaler circuits were characterized with on-wafer probing. The maximum input frequency for proper operation with a given bias was determined and is plotted in Fig. 4 for various designs. The results (averaged over several circuits) show that the LDE designs result in lower P_{diss} than the baseline

design. Without any modifications to the baseline circuit, the LDE HBT, in a drop-in application, can reduce the power dissipation by as much as 50% when compared at 1.5-GHz operation (from 250 to 125 mW). Simulations show that further reduction in $P_{\rm diss}$ can be achieved by optimizing the circuit for the LDE HBT.

IV. Conclusion

In this work, $C_{\rm be}$ reductions are achieved with novel modifications of the baseline TRW HBT by introducing the LDE and δ-doping. This improves both $f_{\rm t}$ and β at low $J_{\rm c}$, and allows for reduced $P_{\rm diss}$ without sacrificing performance. The microwave and dc characteristics of two LDE designs are evaluated. The low-power characteristics of the LDE HBT were evaluated in a programmable 128/129 prescaler designed for the baseline TRW HBT and laid out for a MMIC process. The LDE designs allowed for a dramatic reduction in $P_{\rm diss}$ without any circuit modifications.

Acknowledgment

The authors would like to thank T. Block at TRW for MBE growths and C. Sieg-Fostvelt for layouts.

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